

REMARKS

Claims 1, 2, 7, 8, 11, 12, 14, 15, 20, 21, 24, 25, 30, 31, 37, 38, 43, 44, 47, 48, 53, 54 and 57-96 are pending in this application, with claims 1, 2, 7, 8, 57, 61, 65, 70, 75, 80, 85 and 91 being independent. Claims 1, 2, 7, 8, 14, 15, 20, 21, 24, 25, 30, 31, 57, 58, 61, 62, 67, 70, 72, 75-77, 80-82, 85-88 and 91-94 have been amended. In particular, independent claims 1, 2, 57, and 61 have been amended to recite "the first potential is one of a high level and a low level of the digital signal." Support for this amendment is found in the application, for example, at least on page 14, lines 20-24 and Fig. 7. Independent claims 7 and 8 have been amended to eliminate the term "means" from "capacitor means." Independent claim 70 has been amended to correct a typographical error. Independent claims 75 and 80 have been amended to recite "the at least first and second data latch circuits are connected to the shift register" and "the first potential is one of a high level and a low level of the digital signal," and independent claims 85 and 91 have been amended to recite "the at least first and second data latch circuits are connected to the shift register." Support for this amendment may be found in the application, for example, at least on page 14, lines 20-24; Fig. 7; page 18, lines 12-20; and Fig. 5. No new matter has been introduced.

Applicants acknowledge with appreciation the Examiner's allowance of claims 7, 8, 11, 12, 43, 44, 53, 54, 65, 66, 68-71, 73 and 74, and the Examiner's indication that claims 20, 21, 30, 31, 67, 72 and 85-96 are directed to allowable subject matter if rewritten to overcome the indefiniteness rejections set forth in the Office Action. Claims 20, 21, 30, 31, 67, 72 and 85-96 have been rewritten to address the Examiner's concerns. Accordingly, applicants respectfully request their allowance.

Claims 75-96 have been objected to for various informalities. Applicants have amended claims 75, 80, 85 and 91 in accordance with the Examiner's suggestions and, therefore, respectfully request reconsideration and withdrawal of this objection.

Claims 14, 15, 20, 21, 24, 25, 30, 31, 58, 62, 67, 72 and 75-96 have been rejected as being indefinite. Specifically, with respect to claims 14, 15, 20 and 21, the Examiner stated that the recitation "a first sampling pulse from a first circuit of a preceding stage" and the recitation "a second sampling pulse from a second circuit of a present stage" are unclear. Applicants have amended claims 14, 15, 20 and 21 to address the Examiner's concerns.

With respect to claims 24, 25, 30, 31, 58, 62, 67, 72, 77, 82, 88 and 94, the Examiner stated that the recitation "the potential difference of a power supply" is unclear and lacks antecedent basis. Applicants have amended claims 24, 25, 30, 31, 58, 62, 67, 72, 77, 82, 88 and 94 to address the Examiner's concerns.

With respect to claims 75-96, the Examiner stated that the claims are indefinite for omitting a connection between the recited shift register and the recited at least first and second data latch circuits. Applicants have amended claims 75, 80, 85 and 91 to address the Examiner's concerns.

With respect to claims 76, 81, 87 and 93, the Examiner stated that the recitations "of a preceding stage" and "of a present stage" are unclear. Applicants have amended claims 76, 81, 87 and 93 to address the Examiner's concerns.

In view of the above-listed amendments to the claims, applicants respectfully request reconsideration and withdrawal of the rejection of claims 14, 15, 20, 21, 24, 25, 30, 31, 58, 62, 67, 72 and 75-96.

Independent claims 1, 2, 57 and 61, along with their dependent claims 14, 15, 23, 25, 37, 38, 47, 48, 58-60 and 62-64, have been rejected as being anticipated by Tam (U.S. Patent Number 6,628,146). Applicants have amended claims 1, 2, 57 and 61 to obviate this rejection.

Each of claims 1 and 57, as amended, recites a data latch circuit that samples a digital signal and includes a capacitor having first and second electrodes and a switch. The switch is turned ON and a first potential is input to the second electrode of the capacitor during a reset period, with the first potential being "one of a high level and a low level of the digital signal."

Each of claims 2 and 61, as amended, recites a data latch circuit that samples a digital signal and includes a capacitor having first and second electrodes and a first switch and a second switch. The switches are turned ON to input a first potential to the second electrode of the capacitor during a reset period, with the first potential being "one of a high level and a low level of the digital signal."

Applicants request reconsideration and withdrawal of the rejection of claims 1, 2, 57, and 61, and their dependent claims, because Tam does not describe or suggest the recited data latch circuit having a switch or switches that are turned ON during a reset period to input a first

potential to an electrode of a capacitor, where the first potential is one of a high level or a low level of a digital signal sampled by the data latch circuit.

Tam discloses a TFT CMOS comparator circuit that the Examiner equates to the recited data latch circuit. The comparator circuit receives two voltage signal inputs: VIN1 and VIN2, which the Examiner equates to the recited digital signal. The comparator circuit includes transistors Q6 and Q10, which the Examiner equates to the recited switches, a transistor Q8, and a capacitor C2, which the Examiner equates to the recited capacitor. The capacitor C2 has a right electrode and a left electrode, which the Examiner equates to the recited first and second electrodes, respectively.

When a reset signal RST1 is applied to the gates of transistors Q6 and Q8, both transistors Q6 and Q8 are turned ON and the left electrode of capacitor C2 is connected to ground through transistor Q8. Accordingly, when the transistor Q6 is turned ON, the left electrode of capacitor C2 is driven to ground, rather than to a first potential that is one of a high level or a low level of VIN2 (which, as shown in Figs. 4 and 5, takes on a low value of approximately .5 volts and a high value of approximately 1.5 volts).

Transistor Q10 is not turned ON during a reset period. Rather, it is turned on when a start signal GO1 is applied to its gate. Moreover, even if transistor Q10 and transistor Q6 were turned on simultaneously by a concurrent input of the reset signal RST1 and the start signal GO1, the left electrode of the capacitor C2 would be driven to ground, rather than to a first potential that is one of a high level or a low level of VIN2.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 1, 2, 57, and 61, and their dependent claims 14, 15, 23, 25, 37, 38, 47, 48, 58-60, and 62-64.

Independent claims 75 and 80, along with their dependent claims 76-79 and 81-84, have been rejected as being unpatentable over Koyama (U.S. Publication No. 2002/0021295) in view of Tam and as being unpatentable over Koyama in view of Nakamura (U.S. Publication No. 2002/0075211). Applicants have amended claims 75 and 80 to obviate these rejections.

Claim 75, as amended, recites at least first and second data latch circuits that sample a digital signal and each include a capacitor having first and second electrodes and a switch. The switch is turned ON and a first potential is input to the second electrode of the capacitor during a

reset period, with the first potential being “one of a high level and a low level of the digital signal.”

Claim 80, as amended, recites at least first and a second data latch circuits that sample a digital signal and each include a capacitor having first and second electrodes and a first switch and a second switch. The first switch and the second switch are turned ON to input a first potential to the second electrode of the capacitor during a reset period, with the first potential being “one of a high level and a low level of the digital signal.”

Applicants request reconsideration and withdrawal of the rejection of claims 75 and 80, and their dependent claims, because neither Koyama, Tam, Nakamura, nor any proper combination of the three describes or suggests the recited data latch circuit having a switch or switches that are turned ON during a reset period to input a first potential to an electrode of a capacitor, where the first potential is one of a high level or a low level of a digital signal sampled by the data latch circuit.

The Examiner states that Koyama does not disclose a data latch circuit having the recited switches and capacitor. The Examiner refers to Tam and Nakamura as each independently disclosing these features.

As described above, Tam does not describe or suggest a data latch circuit having the recited switches and capacitor and, therefore, does not remedy the failure of Koyama to describe or suggest this feature. As described below, Nakamura also fails to describe or suggest this feature.

Nakamura describes a level shifter, which the Examiner equates to the recited data latch circuit, that receives a voltage signal IN, which the Examiner equates to the recited digital signal. The level shifter includes switches SW3 and SW1, which the Examiner equates to the recited switches, and a capacitor C2, which the Examiner equates to the recited capacitor. Capacitor C2 includes a right electrode and a left electrode, which the Examiner equates to the recited first and second electrodes, respectively. When the switch SW1 is turned ON, the left electrode of capacitor C2 is set to 1.65 volts, rather than to a first potential that is one of a high level or a low level of voltage signal IN (which, as shown in Fig.14, takes on a low value of approximately .3 volts and a high value of approximately 2.9 volts). Similarly, when both switches SW1 and SW3

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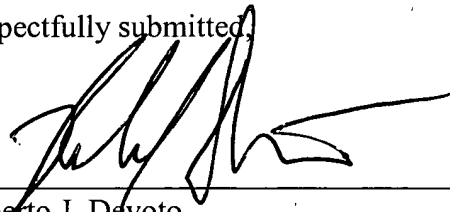
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are turned ON, the left electrode of capacitor C2 is still set to 1.65 volts, rather than to a first potential that is one of a high level or a low level of voltage signal IN.

For at least these reasons, applicants request reconsideration and withdrawal of the rejection of claims 75 and 80, and their dependent claims 76-79 and 81-84.

Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,



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